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Single Supply Multi-V_{th} Level Converters

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Abstract—*The most effective technique to reduce power consumption without degrading the operating speed is to use multiple supply (Multi-V_{DD}) voltage. But, for using Multi-V_{DD} in a circuit, we need to insert a level converter between a low voltage driver and a full swing receiver in order to prevent the large flow of static current for low to high conversion circuit. The application of Multi-V_{DD} system requires two voltage regions, low voltage (V_{DDL}) and high voltage (V_{DDH}) which makes its placement difficult in a circuit. In this paper, we have proposed two new Single Supply (V_{DDH}) Multi Threshold (V_{th}) Level Converters which provide the level up conversions for different values of input voltage. Since the proposed level converters use only single supply voltage it reduces the physical design complexity and can be placed anywhere in the circuit. The performance of these level converters is compared with the previously published Single Supply Multi Threshold Level Converter in terms of power consumption, delay and power delay product (PDP) using Cadence Virtuoso tool in UMC 180nm standard CMOS technology. The proposed level converters perform better than the previously published level converter by offering up to 7.52~66.72% delay reduction and up to17.59~ 64.80% less PDP.*

Index Terms*:* Level Converter, Multi threshold voltage, Single V_{DD} System, Power Delay Product (PDP).

1. INTRODUCTION

With the rapid scaling of technology going on, maintaining both speed and power consumption with each new generation of technology has become a major concern for very large scale integration (VLSI) circuits and system design. Also, with the increase in the usage of battery operated devices like laptops, smart phones, etc., reducing power consumptions in these devices have become the main concern because of the limited lifetime of the battery. The ongoing shrinkage of device size and the addition of increasing important function on the Integrated Circuits (IC) had led to increase the power consumption and thereby increasing the packaging and cooling size.Many techniques had been proposed till now by the several researchers to reduce power consumption. One of the effective techniques to reduce power consumption in CMOS VLSI design is to scale the supply voltage as it results in a quadratic reduction in dynamic power consumption and an exponential reduction in leakage power consumption [1]. CMOS power is divided into three parts, namely leakage power, short circuit power and dynamic power, where dynamic power has been the dominant source. The power consumption of all the components in a circuit can be reduced by scaling the supply voltage, but it also leads to degradation of speed.

To maintain the operating speed while reducing the power consumption, a multi-V_{DD} system that uses more than one V_{DD} was proposed[1].In this approach the circuit is divided into critical and non-critical paths, the critical path is operated with high supply voltage(V_{DDH}) for high performance whereas the non-critical path is operated with low supply voltage(V_{DDL}).

The multi-V_{DD} system (shown in Fig. 1) when implemented in CMOS circuits creates a problem when the high supply voltage (V_{DDH}) gate is directly driven by the low supply voltage (V_{DDL}) gate due to the flow of static current from the supply voltage source to ground as the PMOS transistor (encircle region shown in Fig. 1) at V_{DDH} gate cannot be turned-off fully even when a high input voltage is given. The PMOS transistor remains weakly ON due to the fact that $V_{DDL}<V_{DDH}-\%V_{thp}\%$ [3]. This becomes a serious problem in low power CMOS circuits.

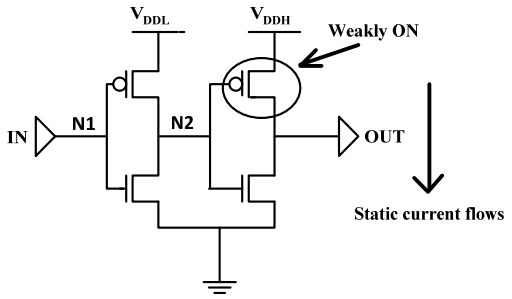

Fig. 1: Direct connection of V_{DDL} gate to V_{DDH} gate.

The level converter plays an important role in the multi-V_{DD} circuit, but the insertion of level converter increases the overall power consumption, delay and area. Moreover, the insertion of level converter also leads to increase the complexity of the circuit and thus results in harder physical

design. Level converter with the Multi-V_{DD} system requires both low voltage (V_{DDL}) and high voltage (V_{DDH}) regions which limit its physical placement to the boundary of V_{DDL} and V_{DDH} voltage islands where, both the voltages are available thereby, restricting its physical design flexibility. To overcome this, we have proposed two new Single Supply Multi Threshold level converters, where only one supply voltage (V_{DDH}) is required to convert the incoming V_{DDL} to the V_{DDH} making its placement much more flexible [2] in the entire higher voltage regions. Since, the proposed level converters require only one supply voltage it can be placed anywhere in the circuit. So, the main aim in the design of level converter is to optimize the overall performance as well as keeping it simple to reduce the complexity of the circuit.

In this paper, the proposed Single Supply Multi threshold Level Converters are compared with the previously published Single Supply Multi threshold Level Converter in terms of their power consumption, delay and PDP using Cadence Virtuoso tool in UMC 180nm standard CMOS technology.

The paper is organized as follows. The previous level converter is shown in Section 2.The operation of two new Proposed Single Supply Multi Threshold Level Converters are discussed briefly in Section 3.The simulation results and comparisons of the level converters in terms of their power consumption, delay and PDP is presented in Section 4. Finally, some conclusions are made in Section 5.

2. PREVIOUS SINGLE SUPPLY MULTI THRESHOLD LEVEL CONVERTER (SMLC)

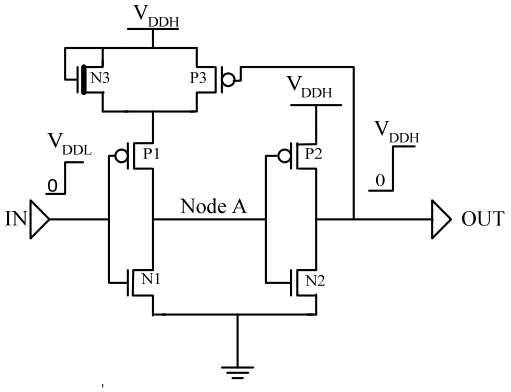

Fig. 2: Existing level converter described in [3]. Thick line in the channel area indicates a high-V_{th} device.

Fig. 2 depicts the previously published Single Supply Multi Threshold Level Converter described in [3].The simulation results of this level converter is given in Table 1 and its comparison with the two new proposed Single Supply Multi Threshold Level Converters is plotted graphically in Figures 5,6 and 7.

3. PROPOSED SINGLE SUPPLY MULTI-THRESHOLD LEVEL CONVERTERS

3(a).Proposed Single Supply Multi-Threshold Level Converter 1 (PSMLC1)

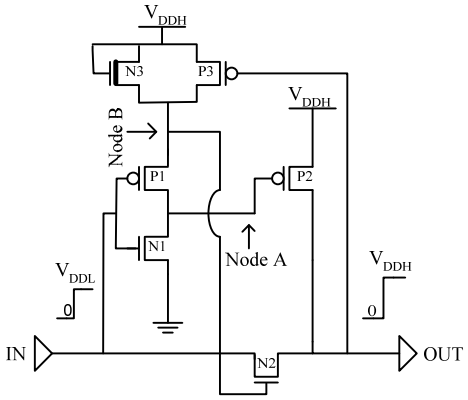

Fig. 3(a): Proposed Single Supply Multi Threshold Level Converter 1 (PSMLC1).Thick line in the channel area indicates a high-V_{th} device.

The circuit diagram of PSMLC1 is shown in Fig. 3(a). The Threshold voltage of N3 (V_{th-N3}) is required to be higher than other transistors in order to avoid static DC current and also it can be adjusted to get the desired virtual V_{DDL} (V_{DDH}-V_{th-N3}). Both PMOS (P1) and NMOS (N1) transistors are provided a virtual low supply voltage V_{DDL} (V_{DDH}-V_{th-N3}) by the diode connected load NMOS (N3) transistor. P3 is a feedback transistor used for pulling up the Node B to V_{DDH} in order to avoid leakage. Pass transistor gate N2 is directly driven by the virtual supply voltage V_{DDL}. PSMLC1 operates as follows. When 0V is given in the input, then P1 is turned ON and N1 is turned OFF. Now the Node A will be pulled high to virtual V_{DDL} so P2 will be off. Pass transistor N2 will pass the output as 0V.The feedback transistor P3 is turned ON which pulls up the internal node B to V_{DDH} thus, compensating the threshold drop created by the diode connected load N3.Now, when V_{DDL} is given as an input, P1 is turned OFF and N1 is turned ON and also the output node is initially charged to V_{DDL}-V_{th-N2} through pass transistor N2. After low to high transition of input, Node A will be pulled down to 0V, thus turning ON P2 and pulling the output node high all way up to V_{DDH}. Pass transistor N2 will be off. In this circuit, both P2 and N2 transistors assist in pulling up the output node high to V_{DDH}. So, the current contention is more and thus increasing the power consumption. The input to output propagation path is small thereby, reducing delay.

3(b).Proposed Single Supply Multi-Threshold Level Converter 2 (PSMLC2)

Fig. 3(b) shows the circuit configurations of proposed Single Supply Multi-Threshold Level Converter 2 (PSMLC2). The Threshold voltage of N3 (V_{TH-N3}) has to be more than other

transistors in order to avoid static DC current and also it can be adjusted to get the desired virtual V_{DDL} (V_{DDH}-V_{th-N3}). Both PMOS (P1) and NMOS (N1) transistors are provided a virtual low supply voltage V_{DDL} (V_{DDH}-V_{th-N3}) by the diode connected load NMOS (N3) transistor.P3 is a feedback transistor used to pull up the Node B to V_{DDH} for avoiding leakage. Pass transistor N2 is driven by node A unlike by virtual low supply voltage V_{DDL} as shown in PSMLC1.The PSMLC2 operates as follows. When an input signal is at 0V, P1 is turned ON and N1 is turned OFF. Node A will be pulled high to V_{DDL} ,thus turning OFF P2 and turning ON N2.The output node will be discharged to 0 V through the pass transistor N2.The feedback transistor P3 is turned ON which pulls up the internal node B to V_{DDH} thus compensating the threshold drop created by the diode connected load N3.Now, when V_{DDL} is given as an input then node A will be pulled down to 0 V and thus turning OFF N2 and turning ON P2.The output will be pulled high all up to V_{DDH} through P2.Pass transistor N2 will be turned OFF. Since, only P3 assist the output from low to high transition, current contention is removed in this circuit which was seen in PSMLC1 thereby, further reducing power consumption.

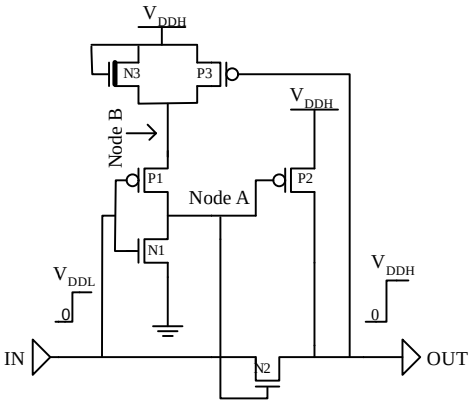

Fig. 3(b): Proposed Single Supply Multi Threshold Level Converter 1 (PSMLC2).Thick line in the channel area indicates a high-V_{th} device.

4. SIMULATION RESULTS AND COMPARISON

All the circuits shown here are designed and simulated using Cadence Virtuoso tool in UMC 180nm standard CMOS technology for the following values of V_{DDL}: 1.2V and 1V.The high supply voltage (V_{DDH}) used for implementation is 1.8V as it is the most ideal voltage in this CMOS technology. Table 1 shows the simulation results of the level converters in terms of their power consumption, delay and PDP. Comparison between level converters is plotted graphically in Figures 5, 6 and 7.

Table 1: Comparison of Level Converters in terms of their power consumption, delay and PDP.

VDDL	Level Converter	Power (µW)	Delay (ps)	PDP (fJ)
1.2	SMLC	1.716	135.58	0.233
	PSMLC1	1.828	45.13	0.082
	PSMLC2	1.530	125.37	0.192
1	SMLC	1.797	144.43	0.260
	PSMLC1	1.947	53.04	0.103
	PSMLC2	1.575	131.75	0.207

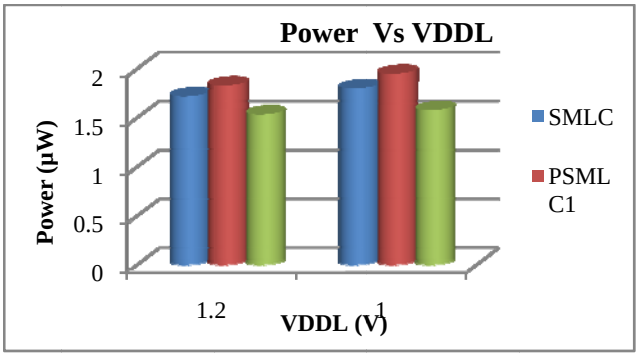

Fig. 4: Plot for Power Vs V_{DDL} for different level converters.

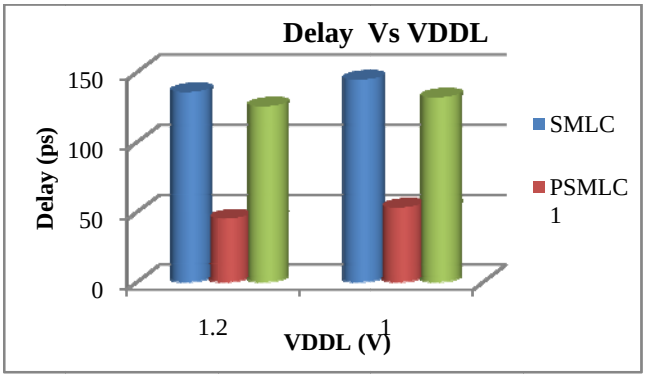

Fig. 5: Plot for Delay Vs V_{DDL} for different level converters.

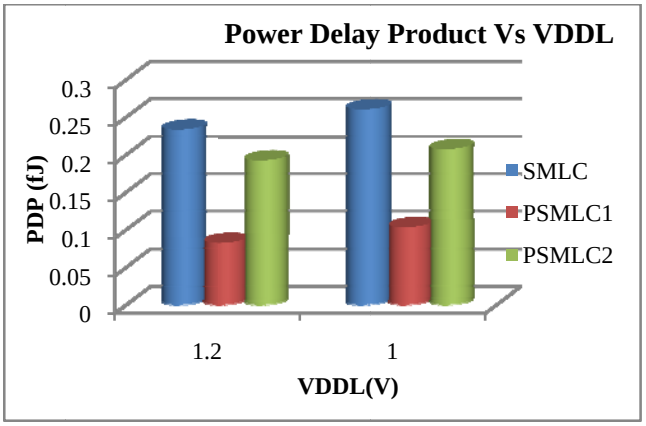

Fig. 6: Plot for PDP Vs V_{DDL} for different level converters.

5. CONCLUSION

In this paper, we have proposed two new level converters which require only one power-supply voltage (V_{DDH}) and provides the level up conversions for the various levels of input voltages (1.2V and 1V).Both the proposed level converters are compared with the previously published level converter in terms of their power consumption, delay and PDP for different values of input voltages. From the simulation Table 1 we can see that PSMLC1 are 63.28~ 66.72 % and 59.74~64.00% faster than both SMLC and PSMLC2 respectively. The power consumption of PSMLC1 are 6.12~7.70 % and 16.30~19.10 % higher than both SMLC and PSMLC2 respectively, due to the contention current as discussed in Section 3.The power consumption and delay of PSMLC2 are 10.84~12.35% and 7.52~8.77% lower than SMLC. Both PSMLC1 and PSMLC2 provides 60.38~64.80% and 17.59~20.38% less PDP than previously published level converter (SMLC). Both the proposed circuits maintain higher speed characteristics as compared to the previously published level converter.

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